Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

1. (Currently Amended) A system comprising:

a processor;

C1

a detector to detect a power management event; and

a controller to transition, in response to the power management event, a first setting of the processor from a first performance mode to a second performance mode, including to raise a processor supply voltage level from a first voltage level to a second voltage level, and then to raise the processor clock frequency from a first frequency level to a second frequency level, the processor to remain in an active mode during the voltage level transition, wherein during the frequency level transition the processor is to be placed in a sleep state of and not a deep sleep state, a core processor clock remains active during the sleep state.

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Previously presented) The system of claim 4, wherein a system clock input to the processor remains active during the sleep state.

8. (Original) The system of claim 1, wherein the power management event includes a change of the system power source from an internal power source to an external power source.

9. (Previously presented) The system of claim 1, wherein the voltage level transition requires 5-500 microseconds.

10. (Previously presented) The system of claim 1, wherein the frequency level transition requires less than 5 microseconds.

11. (Currently Amended) A system comprising:

a processor;

a detector to detect a power management event;

a controller to transition the processor, in response to the power management event, ~~the transition included~~ to lower ~~the~~ a core processor clock frequency from a first frequency to a second frequency, and to lower ~~the~~ a core processor supply voltage level from a first voltage level to a second voltage level, the processor to remain in an active mode during the voltage level transition, wherein during the frequency level transition the processor is to be placed in a sleep state of and not a deep sleep state, the core processor clock to remain active during the sleep state.

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Previously presented) The system of claims 13, wherein a system clock input to the processor remains active during the sleep state.

17. (Canceled)

18. (Original) The system of claim 11, wherein the power management event includes a change of the system power source from an external power source to an internal power source.

19. (Previously presented) The system of claim 12, wherein the frequency level transition requires less than 5 microseconds.

20. (Previously presented) The system of claim 11, wherein the voltage level transition requires 50 - 500 microseconds.

21. (Currently Amended) A computer-readable medium having stored thereon a set of instructions to translate instructions, the set of instructions, which when executed by a processor, cause the processor to perform a method comprising:

detecting a power management event;

raising a processor supply voltage level from a first voltage level to a second voltage level, the processor to remain in an active mode during voltage level transition,

~~then~~ raising the processor clock frequency from a first frequency level to a second frequency level, wherein during the raising of the frequency level, the processor is to be placed in a sleep state of and not a deep sleep state, and a core processor clock remains active during the sleep state,

if the power management event includes the system power source switching from an internal power source to an external power source; and

lowering a core processor clock frequency from a first frequency to a second frequency;

lowering a core processor supply voltage level from a first voltage level to a second voltage level, the processor remaining in an active mode during voltage level transition

if the power management event includes the system power source switching from an external power source to an internal power source.

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Canceled)

C1

29. (Previously presented) The computer-readable medium of claim 25, wherein a system clock input to the processor remains active during the sleep state.

30. (Canceled)

31. (Currently Amended) An apparatus comprising:

a detector to receive an indication to change power states in the system; and

a controller, in response to the indication, to raise a processor supply voltage level from a first voltage level to a second voltage level, and then to raise the processor clock frequency from a first frequency level to a second frequency level, the processor to remain in an active mode during the voltage level transition, wherein during the frequency level transition the processor is to be placed in a sleep state of and not a deep sleep state, a core processor clock remains active during the sleep state.

32. (Currently Amended) The apparatus of claim 31, wherein during the frequency level transition ~~the processor to be placed in a sleep state and not a~~

~~deep sleep state, and core component clock and~~ a system clock input to the processor is to remain active during the sleep state.

33. (Original) The apparatus of claim 31, wherein the indication is generated in response to a change in a power source in the system from an internal power source to an external power source.

34. (Currently Amended) An apparatus comprising:

a detector to receive an indication to change power states in the system; and

a controller, in response to the indication, to lower a core processor clock frequency from a first frequency to a second frequency, and to lower a core processor supply voltage level from a first voltage level to a second voltage level, the processor to remain in an active mode during the voltage level transition, wherein during the frequency level transition the processor is to be placed in a sleep state of and not a deep sleep state, a core processor clock remains active during the sleep state.

35. (Currently Amended) The apparatus of claim 34, wherein during the frequency level transition ~~the processor to be placed in a sleep state and not a deep sleep state, and the core component clock and~~ a system clock input to the component is to remain active during the sleep state.

36. (Original) The apparatus of claim 34, wherein the indication is generated in response to a change in a power source in the system from an external power source to an internal power source.